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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	08/903486
Filing Date	July 29, 1997
First Named Inventor	Forbes, Leonard
Group Art Unit	2811
Examiner Name	Mintel, W.

Sheet 1 of 1

Attorney Docket No: 00303.326US1

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Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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	US-5393999	02/28/1995	Malhi, S.	257	289	06/09/1994
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Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
DHK	JP-57-126175	08/05/1982	Hamakawa, Y., et al	H01L	31/04	
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
nm		BURNS, S.G., et al., In: <u>Principles of Electronic Circuits</u> , West Publishing Co., St. Paul, MN, (1987), 382-383	
		BURNS, S., et al., In: <u>Principles of Electronic Circuits</u> , West Publishing Company, (1987), pp. 380	
		CAPASSO, F., et al., "New Floating-Gate AlGaAs/GaAs Memory Devices with Graded-Gad Electron Injector and Long Retention Times", <u>IEEE Electron Device Letters</u> , (1988), pp. 377-379	
		NG, K., In: <u>Complete Guide To Semiconductor Devices</u> , McGraw-Hill, Inc. New York, (1995), pp. 322-328, 605-608	
		WOLF, S., "Semiconductor Memory Process Integration", <u>Silicon Processing for The VLSI Era, Volume 2: Process Integration</u> , (1990), pp. 623-628	

EXAMINER

Donghee Kang

DATE CONSIDERED

7-17-03

Substitute Disclosure Statement Form (PTO-1449)

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